

2521/203, 2602/202
2601/202, 2603/202
DIGITAL AND ANALOGUE
ELECTRONICS II
June/July 2020
Time: 3 hours



THE KENYA NATIONAL EXAMINATIONS COUNCIL

**DIPLOMA IN ELECTRICAL AND ELECTRONIC ENGINEERING
(POWER OPTION)
(TELECOMMUNICATION OPTION)
(INSTRUMENTATION OPTION)
MODULE II**

DIGITAL AND ANALOGUE ELECTRONICS II

3 hours

INSTRUCTIONS TO CANDIDATES

You should have the following for this examination:

Answer booklet;

Mathematical table/Non-programmable scientific calculator;

Drawing instruments.

*The paper consists of **EIGHT** questions in **TWO** sections, **A** and **B**.*

*Answer any **TWO** questions from section **A** and any **THREE** questions from section **B** in the answer booklet provided.*

All questions carry equal marks.

Maximum marks for each part of a question are as indicated.

Candidates should answer the questions in English.

This paper consists of 8 printed pages.

Candidates should check the question paper to ascertain that all the pages are printed as indicated and that no questions are missing.

SECTION A: ANALOGUE ELECTRONICS II

Answer any **TWO** questions from this section.

1. (a) Figure 1 shows a circuit diagram of an active filter.

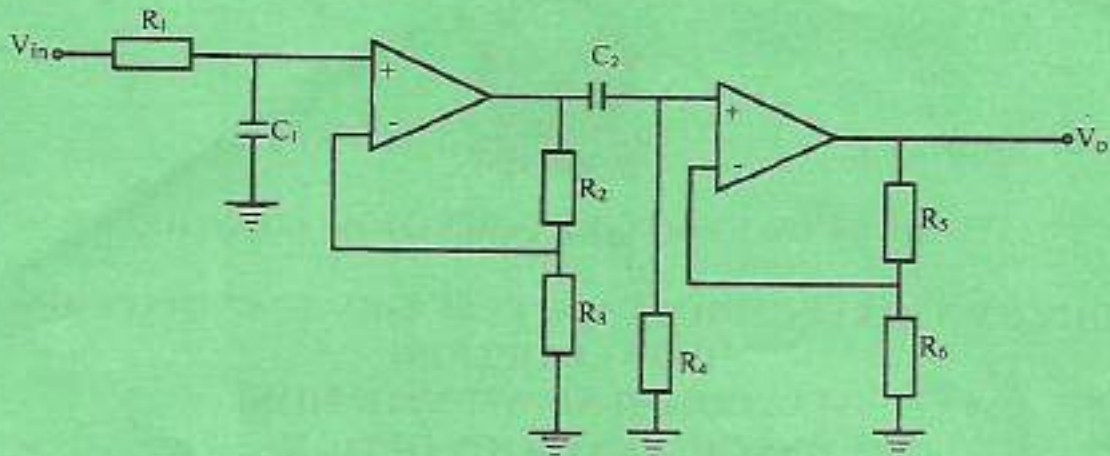


Fig. 1

- (i) identify the type of the filter;
- (ii) draw its labelled frequency response curve;
- (iii) describe its operation.

(7 marks)

- (b) A transistor in a common-base amplifier circuit has the following h-parameter values: $h_{ib} = 28\Omega$; $h_{rb} = -0.98$; $h_{ob} = 5 \times 10^{-4}$; $h_{fb} = -0.34 \times 10^{-6}S$ and load resistance $r_L = 1.21k\Omega$.

Determine the:

- (i) current gain;
- (ii) input resistance;
- (iii) voltage gain.

(9 marks)

- (c) State **four** applications of a triac.

(4 marks)

2. (a) Figure 2 shows a symbol of a semiconductor device.



Fig. 2

- (i) identify the device;
 (ii) explain the operation of the device.

(5 marks)

- (b) The intrinsic stand-off ratio of a unijunction transistor (UJT) is 0.65 and the interbase resistance is $7.5 \text{ k}\Omega$, determine the:

- (i) r_{B1} ;
 (ii) r_{B2} .

(5 marks)

- (c) (i) Define each of the following with reference to thyristors:

(I) break over voltage; *→ volt added without*

(II) peak reverse voltage; *→ max reverse voltage that can be applied without causing physical damage to the device*

- (ii) With the aid of a V-I characteristic curve describe the operation of a silicon controlled rectifier (SCR). *→ also see the mechanism of the device* (10 marks)

3. (a) State two characteristics of a laser light. *→ it is only available within a given area and parallel* (2 marks)

- (b) List two conditions necessary for sustained oscillations in oscillators. (2 marks)

- (c) Figure 3 shows an electric circuit. With the aid of waveforms explain its operation. (6 marks)

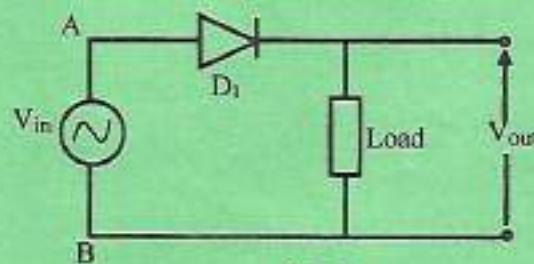


Fig. 3

- (d) (i) With the aid of a circuit diagram describe the operation of a blocking oscillator.
(ii) State two applications of oscillators.

(10 marks)

SECTION B: DIGITAL ELECTRONICS

Answer any **THREE** questions from this section.



- (a) Perform each of the following number system conversions:

- (i) 7562.45_{10} to octal;
(ii) 1938.85_{10} to hexadecimal;
(iii) 11010.111_2 to decimal.

(11 marks)

- (b) (i) Using Boolean algebra simplify the following expressions:

- (I) $ABC + \overline{A}B + ABC$;
(II) $AB + (\overline{A} + \overline{B})C + A$.

- (ii) Convert the binary number 11101 to Gray code.

(9 marks)

5. (a) (i) Define each of the following as applied to analogue to digital converters (ADCs).

- (I) accuracy;
(II) resolution;
(III) conversion time.

- (ii) A 10-bit ramp type analogue to digital converter is driven by a 1 MHz clock. Determine the:

- (I) maximum conversion time;
(II) average conversion time;
(III) maximum rate of conversion.

(8 marks)

(b) An 8-bit digital system uses the following memory address ranges:

0000H - 07FF H : ROM

2000H - 23FF H : RAM

If the available chips are $1\text{ k} \times 8$ ROM and $0.5\text{ k} \times 4$ RAM, determine the:

- (i) size of ROM and RAM in kilobytes;
- (ii) number of chips required for each memory type.

(12 marks)

6. (a) Figure 4 shows a DTL NAND gate circuit. Describe its operation.

(5 marks)

(6) (a) When both D_1 & D_2 have positive voltage applied to them, neither the diode nor current is turned on by the current provided by V_{CC} through R_1 . Since X becomes saturated, point X is brought to zero voltage.

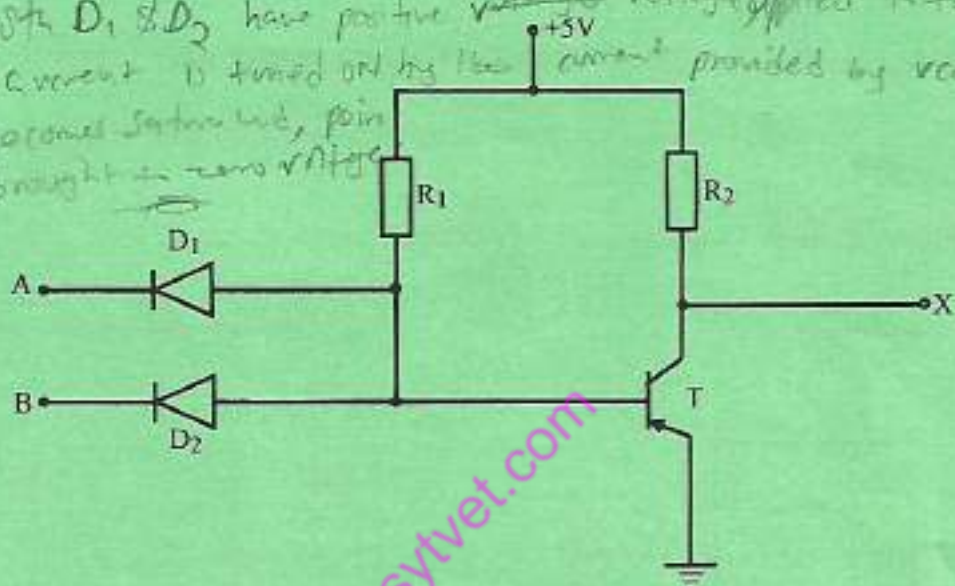


Fig. 4

(b) (i) Define each of the following as applied in sequential circuits:

- (I) set-up time; \rightarrow is the time before trigger
- (II) maximum clocking frequency;
- (III) hold time. \rightarrow is the time after trigger

(ii) A four stage binary ripple counter has a propagation delay of 40 ns in each flip flop. Determine the:

- (I) total propagation delay; $4 \times 40 = 160\text{ ns}$
- (II) maximum operating frequency; $f = \frac{1}{4 \times 40} = \frac{1}{160} = 6.25\text{ kHz}$

(7 marks)



- (c) A security firm intends to install an alarm system with 3 motion sensors A, B and C. To prevent false alarms produced by a single sensor activation, the alarm will be triggered only when at least two sensors are activated simultaneously.
- Draw the truth table for the alarm system;
 - Obtain a simplified Boolean expression of the system using a Karnaugh map.
- (8 marks)

7. (a) (i) Distinguish between synchronous and asynchronous counters.
- (ii) State three applications of binary counters.
- (5 marks)
- (b) (i) Draw a schematic diagram of a 4-bit ring counter using D-type flip flops.
- (ii) Draw the counting sequence waveforms for the counter in b (i).
- (7 marks)
- (c) Figure 5 shows a logic diagram of a binary counter.

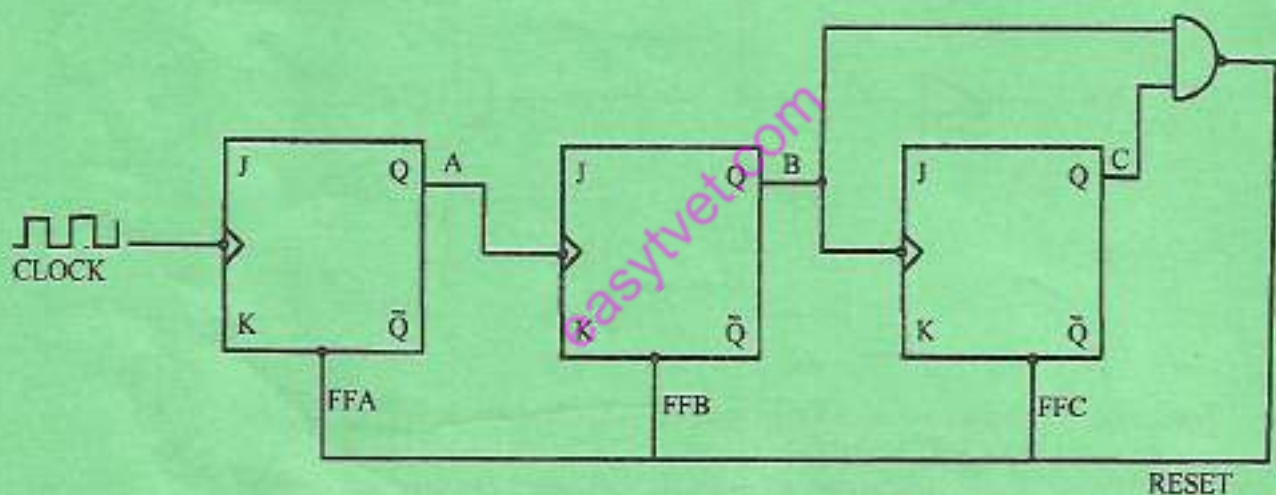


Fig. 5

- Explain its operation;
- Draw the state transition diagram for the counter.

(8 marks)

A	B	C
0	0	0
1	0	1
0	1	0
1	1	1

8. (a) (i) State De-Morgans theorems.
 (ii) Using De-Morgans theorems simplify the expression:

$$F = \overline{(\overline{X \cdot Y})(\overline{Y + Z})}$$

(5 marks)

- (b) (i) Draw the truth table of a half subtractor circuit.
 (ii) Obtain the Boolean expression for the circuit in b.(i)
 (iii) Using logic gates implement the expression obtained in b.(ii)

(9 marks)

- (c) With the aid of a diagram, describe the operation of a CMOS inverter.

(6 marks)

2(a)

(i) Is a reversed biased

(ii) The reversed biased voltage increases the depletion layer widens it increases the dielectric thickness which interns reduce the capacitance when the reverses biased voltage is decreased. The depletion layer narrows down, this decreases the electric thickness which interns increases the capacitance.

2(b)

(i) $\eta = 0.65 - R_{B1} = 75 \text{ k}\Omega$

$R_{B1} \cdot \eta = R_{B2}$

$$\frac{R_{B1} \cdot \eta}{R_{B2}} = 0.65 = \frac{R_{B1}}{7.5}$$

(ii) $7.5 \text{ k}\Omega \cdot 4.875 \text{ k}\Omega$

$= 2.625$

2521/203

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0.65×7.5

7

Turn over

2601/202

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$= 4.875 \text{ k}\Omega$

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